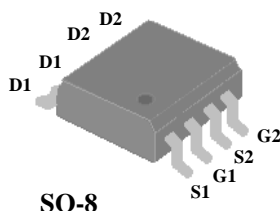


- ▼ Simple Drive Requirement
- ▼ Low On-resistance
- ▼ Fast Switching Performance

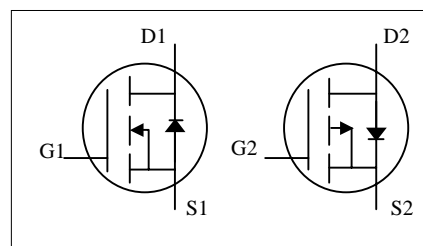


N-CH	$BV_{DSS}$	30V
	$R_{DS(ON)}$	28m $\Omega$
	$I_D$	7A
P-CH	$BV_{DSS}$	-30V
	$R_{DS(ON)}$	50m $\Omega$
	$I_D$	-5.3A

## Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



## Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
$V_{DS}$	Drain-Source Voltage	30	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current <sup>3</sup>	7.0	-5.3	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current <sup>3</sup>	5.8	-4.7	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	20	-20	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation	2		W
	Linear Derating Factor	0.016		W/ $^\circ C$
$T_{STG}$	Storage Temperature Range	-55 to 150		$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150		$^\circ C$

## Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	62.5	$^\circ C/W$


**N-CH Electrical Characteristics @ $T_j=25^{\circ}\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=7A$	-	-	28	$m\Omega$
		$V_{GS}=4.5V, I_D=5A$	-	-	42	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
$g_{fs}$	Forward Transconductance	$V_{DS}=10V, I_D=6A$	-	6	-	S
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=30V, V_{GS}=0V$	-	-	1	$\mu A$
	Drain-Source Leakage Current ( $T_j=70^{\circ}\text{C}$ )	$V_{DS}=24V, V_{GS}=0V$	-	-	25	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_D=6A$	-	8.4	13.5	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=24V$	-	1.4	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	4.7	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>2</sup>	$V_{DS}=20V$	-	5	-	ns
$t_r$	Rise Time	$I_D=1A$	-	8	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	18.5	-	ns
$t_f$	Fall Time	$R_D=20\Omega$	-	9	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	485	770	pF
$C_{oss}$	Output Capacitance	$V_{DS}=25V$	-	80	-	pF
$C_{riss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	75	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=7A, V_{GS}=0V$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time <sup>2</sup>	$I_S=6A, V_{GS}=0V,$	-	19	-	ns
		$di/dt=100A/\mu s$	-	11	-	nC

**P-CH Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-5.3A$	-	-	50	$m\Omega$
		$V_{GS}=-4.5V, I_D=-4.2A$	-	-	90	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-	-3	V
$g_{fs}$	Forward Transconductance	$V_{DS}=-10V, I_D=-5A$	-	5	-	S
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1	$\mu A$
	Drain-Source Leakage Current ( $T_j=70^\circ\text{C}$ )	$V_{DS}=-24V, V_{GS}=0V$	-	-	-25	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_D=-5A$	-	8	13	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=-15V$	-	1.7	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	4.5	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>2</sup>	$V_{DS}=-15V$	-	6.7	-	ns
$t_r$	Rise Time	$I_D=-1A$	-	10	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=-10V$	-	21	-	ns
$t_f$	Fall Time	$R_D=15\Omega$	-	10	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	595	950	pF
$C_{oss}$	Output Capacitance	$V_{DS}=-25V$	-	80	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	75	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=-2.6A, V_{GS}=0V$	-	-	-1.2	V
$t_{rr}$	Reverse Recovery Time <sup>2</sup>	$I_S=-5A, V_{GS}=0V,$	-	18	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	11	-	nC

**Notes:**

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board ; 135 °C/W when mounted on Min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

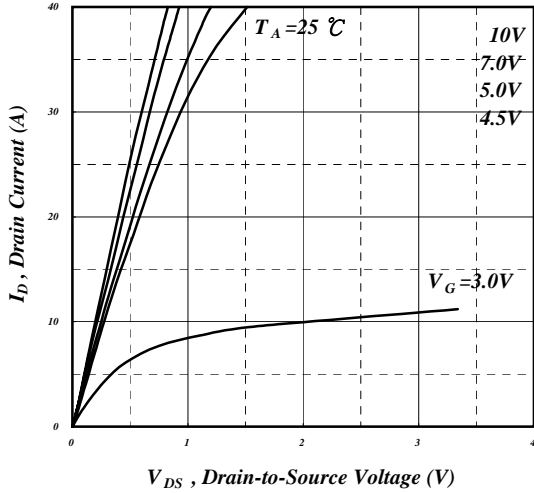
USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

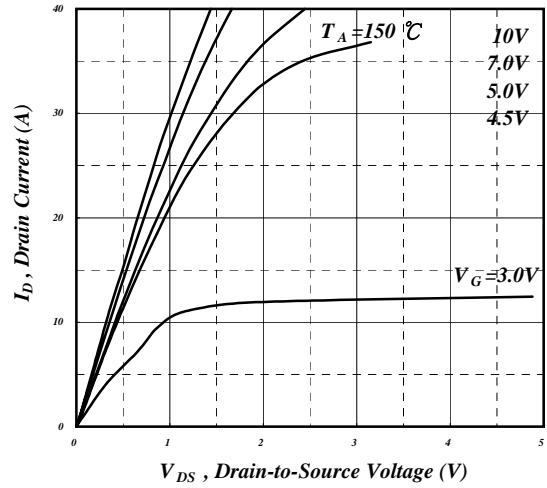
APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



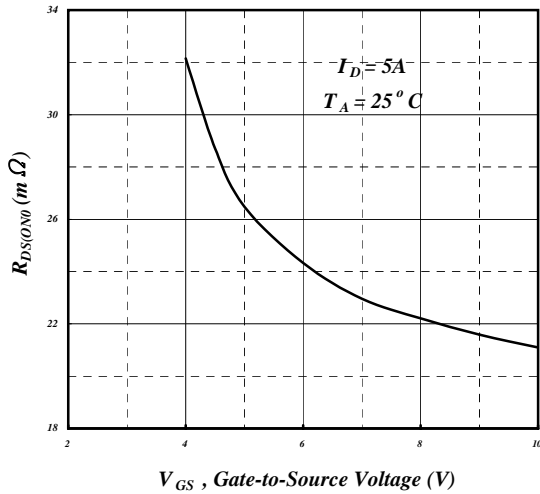
## N-Channel



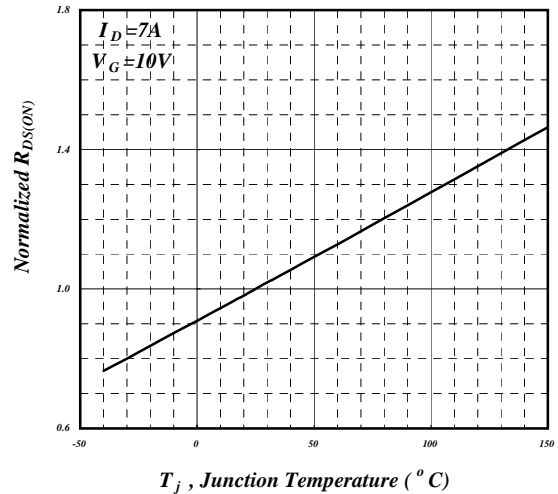
**Fig 1. Typical Output Characteristics**



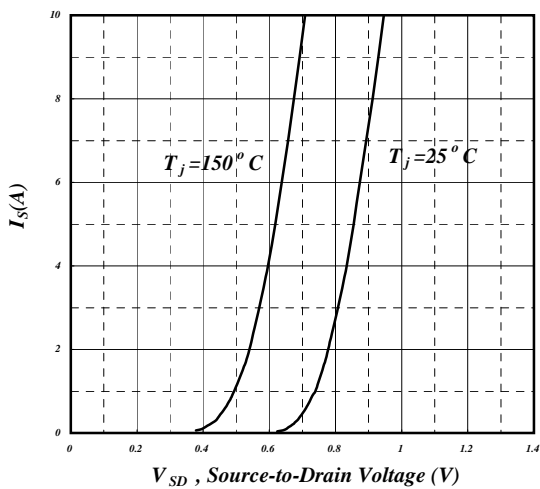
**Fig 2. Typical Output Characteristics**



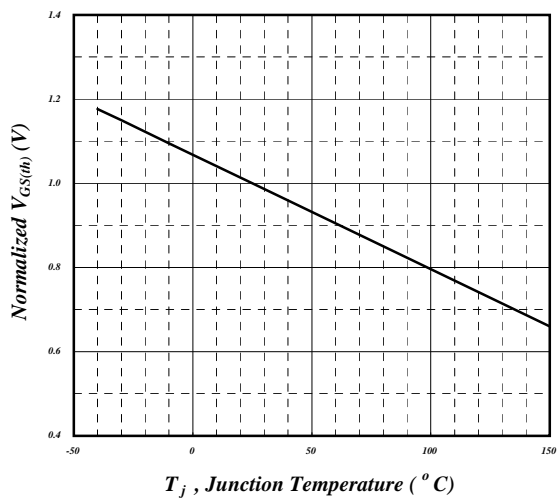
**Fig 3. On-Resistance v.s. Gate Voltage**



**Fig 4. Normalized On-Resistance v.s. Junction Temperature**



**Fig 5. Forward Characteristic of Reverse Diode**



**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**



N-Channel

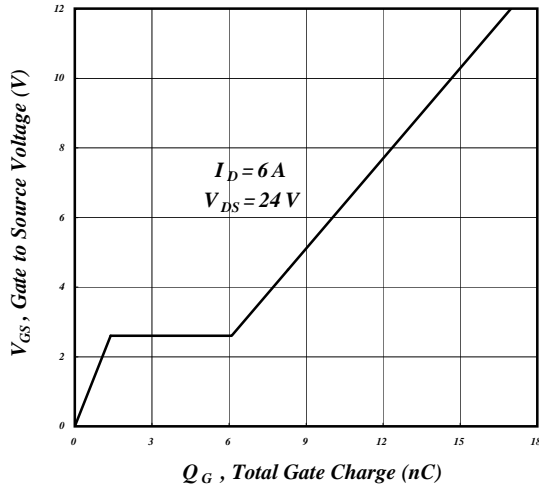


Fig 7. Gate Charge Characteristics

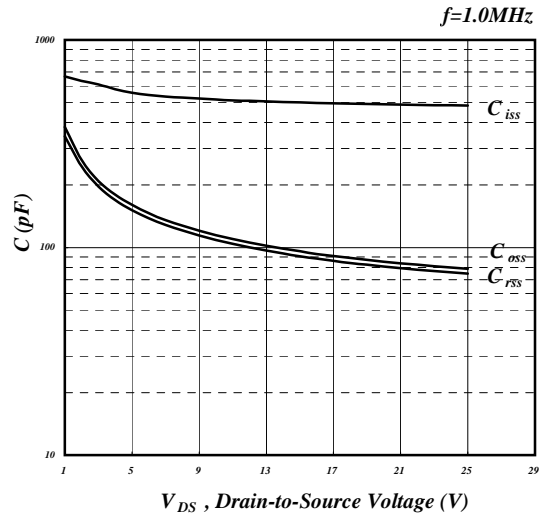


Fig 8. Typical Capacitance Characteristics

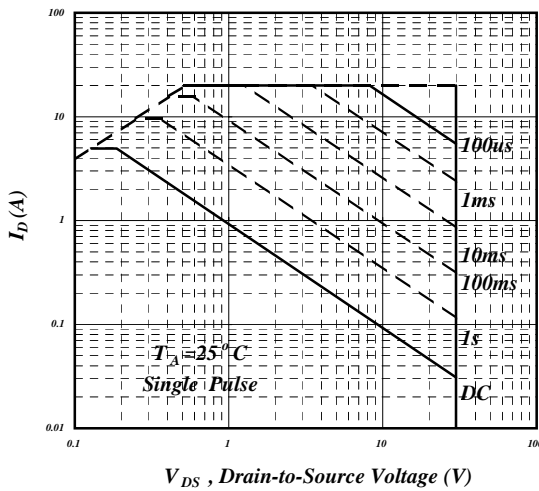


Fig 9. Maximum Safe Operating Area

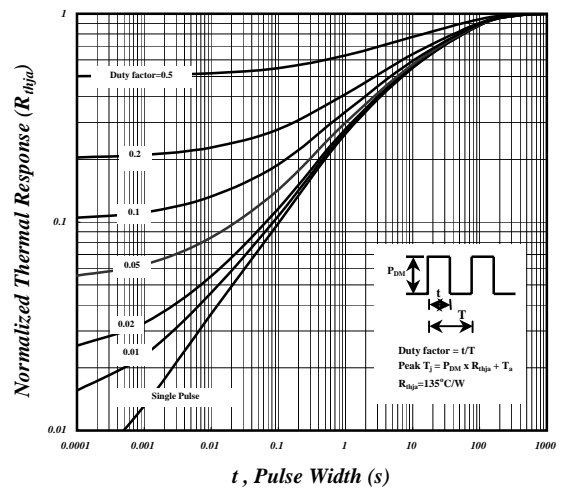


Fig 10. Effective Transient Thermal Impedance

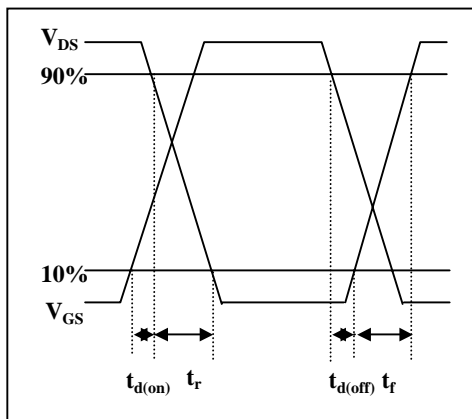


Fig 11. Switching Time Waveform

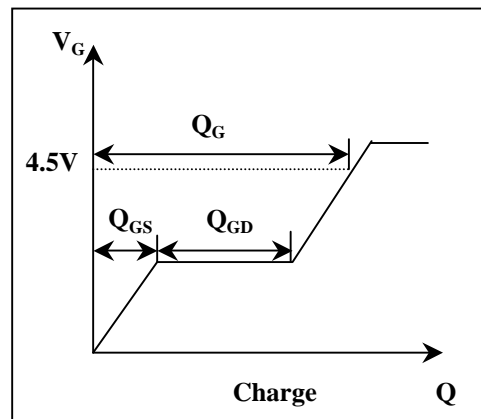


Fig 12. Gate Charge Waveform



# AP4501GM

## P-Channel

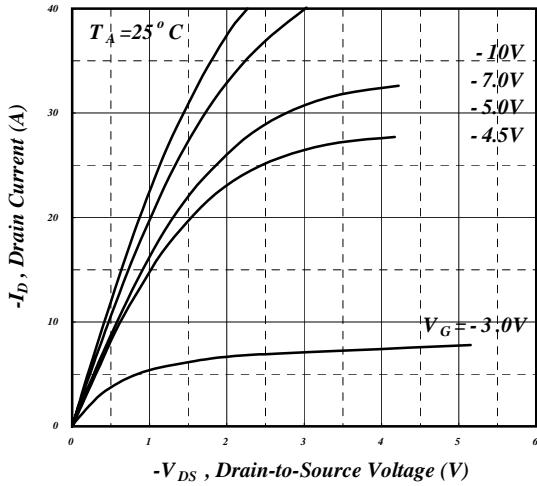


Fig 1. Typical Output Characteristics

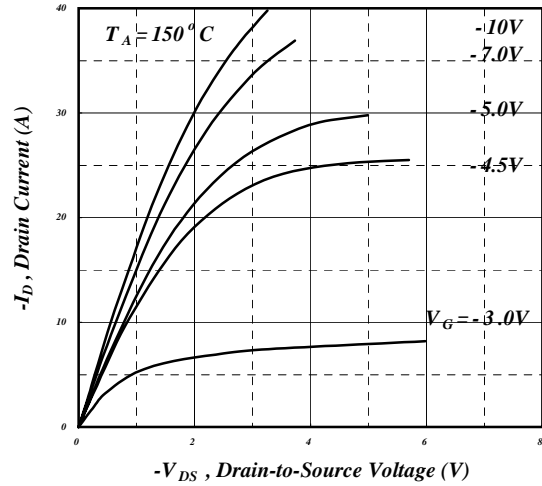


Fig 2. Typical Output Characteristics

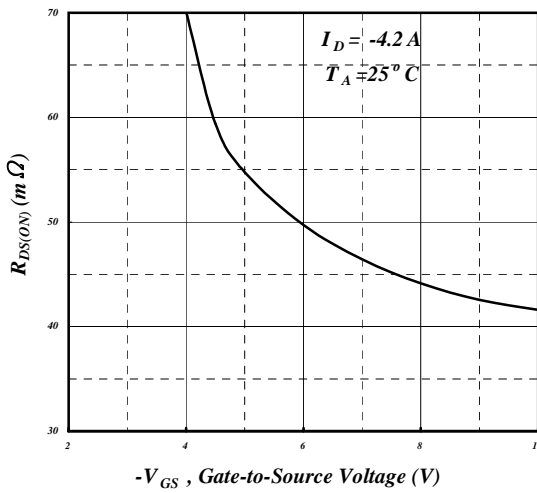


Fig 3. On-Resistance v.s. Gate Voltage

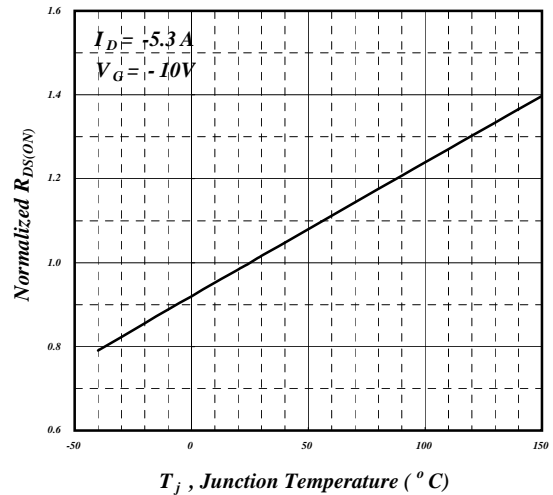


Fig 4. Normalized On-Resistance v.s. Junction Temperature

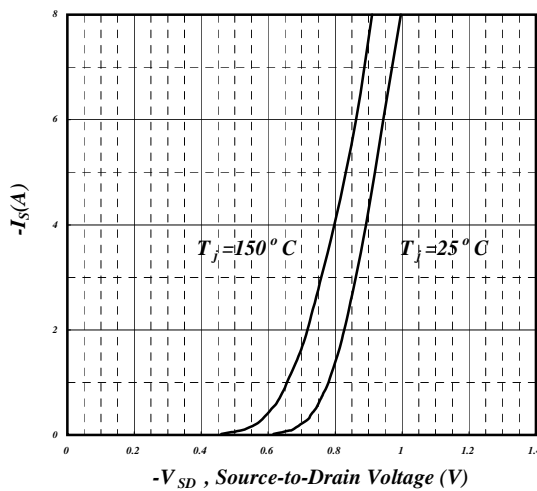


Fig 5. Forward Characteristic of Reverse Diode

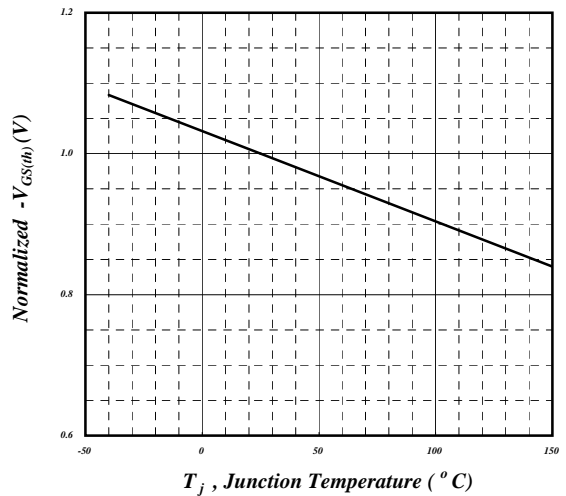


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



P-Channel

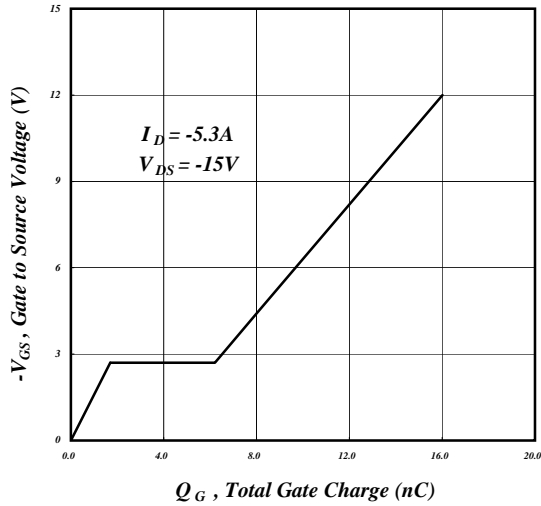


Fig 7. Gate Charge Characteristics

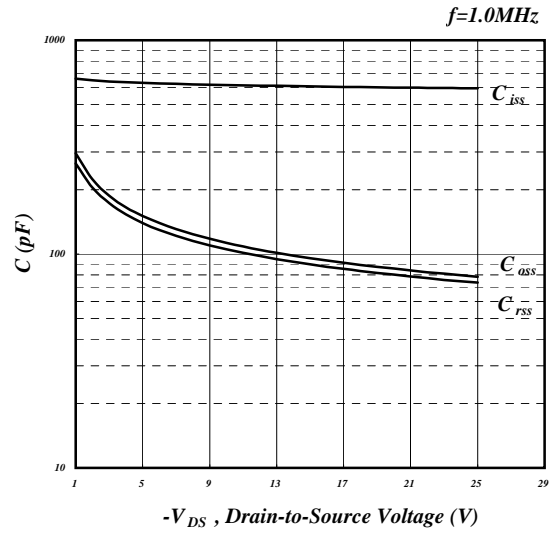


Fig 8. Typical Capacitance Characteristics

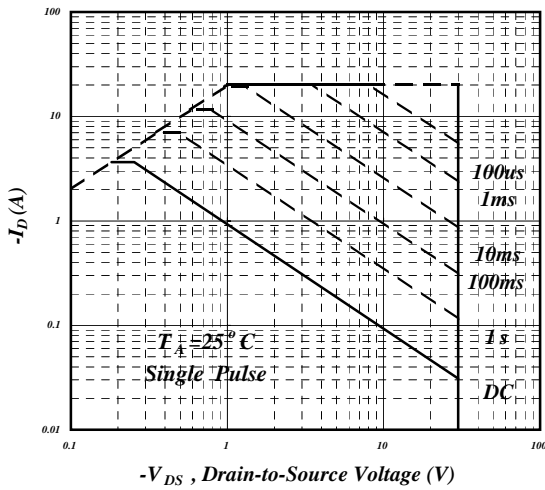


Fig 9. Maximum Safe Operating Area

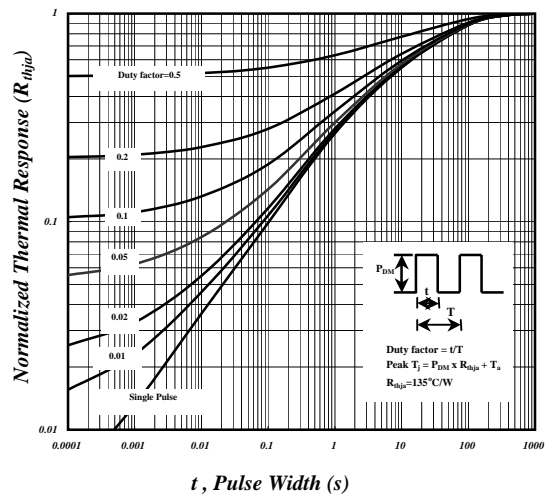


Fig 10. Effective Transient Thermal Impedance

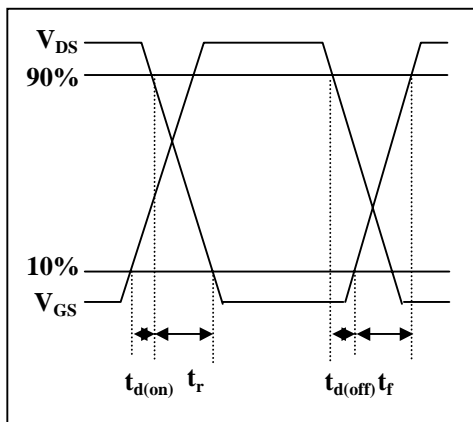


Fig 11. Switching Time Waveform

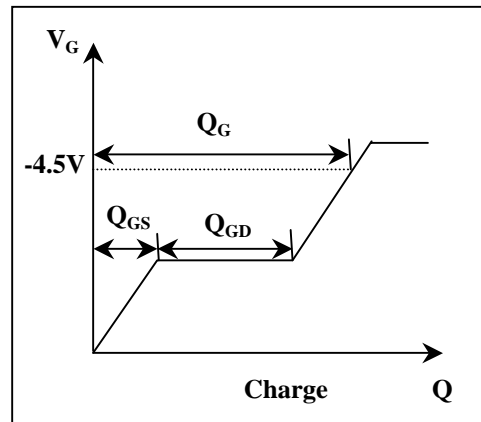
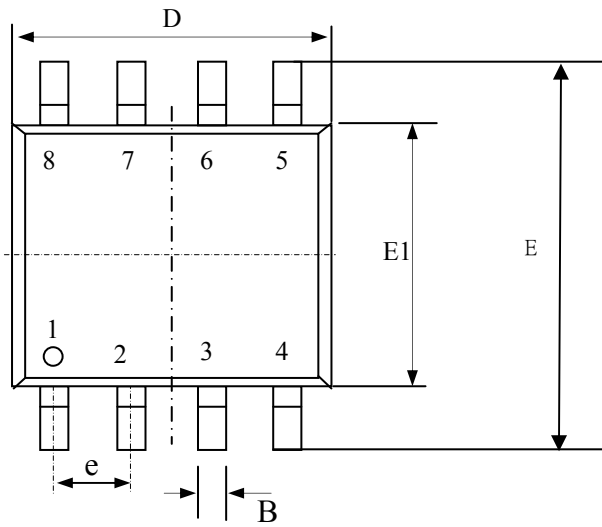


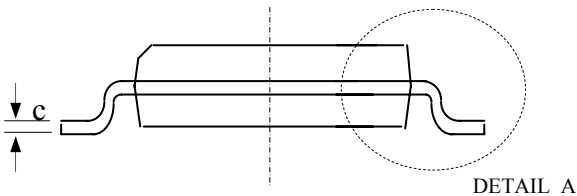
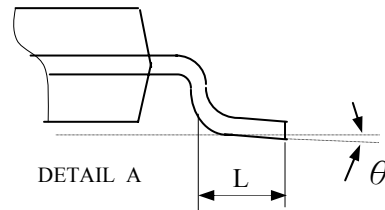
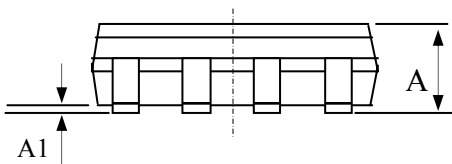
Fig 12. Gate Charge Waveform



Package Outline : SO-8

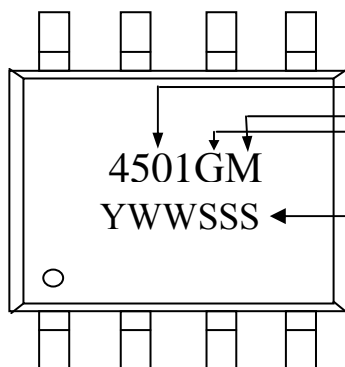


SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
B	0.33	0.41	0.51
C	0.19	0.22	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
E	5.80	6.15	6.50
L	0.38	0.71	1.27
$\theta$	0	4.00	8.00
e	1.27 TYP		



1. All Dimension Are In Millimeters.
2. Dimension Does Not Include Mold Protrusions.

Part Marking Information & Packing : SO-8



Part Number      Package Code  
 meet Rohs requirement

Date Code (YWWSSS)

Y : Last Digit Of The Year

WW : Week

SSS : Sequence